PROCEED Project

Minalogic's PROCEED project was a 4.2 million euros, 24-month project supported by the French *FIU* (*Fond Interministériel Unique*).

Started in 2009, the goal of the PROCEED project was to demonstrate the high alignment accuracy (< 1 µm) of chip-to-wafer structures made by direct metallic bonding. Such structures are required for high performance 3D interconnexion circuits and enable a wide range of applications in microelectronics as well as in optoelectronics or MEMS.

Direct copper-to-copper bonding requires good planarity and excellent surface quality, especially in terms of both particulate and metallic contamination. The low roughness of the copper pillars and pads, as well as the topography between the copper and oxide areas, are critical to obtain good bond strength at low force and room temperature.

The process, based on chip-to-wafer direct metallic bonding, was developed at CEA-Leti to overcome certain limitations in 3D integration. This technology consists of attaching chips on a substrate at low temperature and force, creating a bond of high mechanical and electrical integrity due to local metallic bonding.

ALES supplied technology to support the surface preparation while CEMES-CNRS characterized the bond quality and analysed changes to the copper metallurgy during the annealing step. STMicroelectronics was driving the application of this technology for the high-density 3D integration.

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